Preliminary

10-bit 40MS/s Pipelined-AD-Converter

Features

- Differential Input
- 1.5V Analog/Digital Core Voltage
- Digital Outputs Compatible with 3.3V Logic
- Signal-to-Noise: 58dB@20MHz
- Spurious Free Dynamic Range: 71dB@20MHz
- Internal Reference
- low power consumption 11mW
- power-down mode
- 130 nm CMOS technology
- Operating temperature range: -40 to +85°C

Applications

- Ultrasound
- Portable Instrumentation
- Imaging Systems
- Wireless Communications
- Baseband Digitization

General Description

The 10-bit pipelined analog-to-digital converter provides a maximum sample rate of 40MS/s with low power consumption of 11mW from a core-supply voltage of 1.5V. For power-savings a power-down mode is available. The analog inputs are differential for high noise immunity and allow a large voltage-swing of ±900mV.

The device possesses an internal voltage reference which can be bypassed to use external references to meet higher accuracy requirements of the system.

For data acquisition the IP-core has a parallel tri-state output which works with logic levels of up to 3.3V. In a stand-alone version the ADC contains an SPI interface with internal FIFO for timing-tolerant communication.

Block diagram