12-bit 50kS/s SAR-AD-Converter

Features

- 12-bit 50kS/s SAR ADC
- ultra low power consumption <60µW
- rail-to-rail input voltage range
- separated analog and digital supply at AVDD = 1.5V and DVDD = 1.5V
- internal common mode voltage generation
- DNL / INL < 1 LSB
- SPI Interface with 100 word FIFO buffer
- Pure 130 nm CMOS technology, core cell area: 0.4mm²
- Operating temperature range: –40 – +85 °C

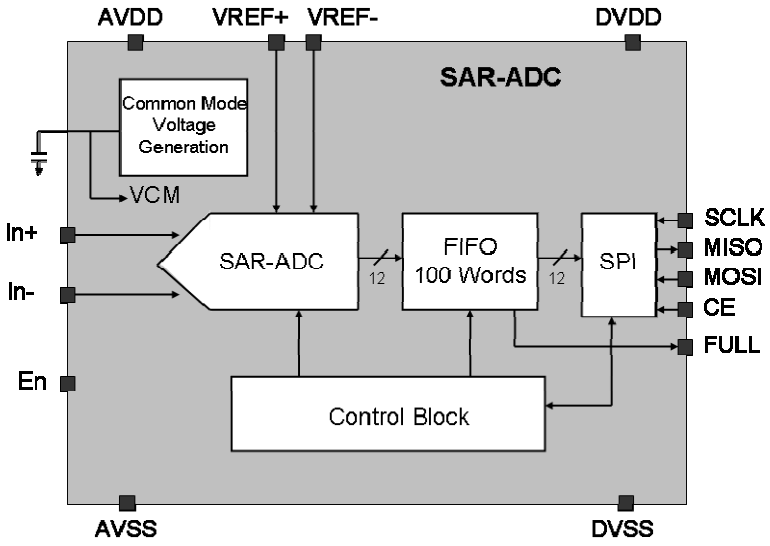
General Description

IMST's 12-bit analog-to-digital converter solution provides a maximum sample rate of 50kS/s with an ultra low power consumption below 60µW at a low supply voltage of 1.5V for both analog and digital part. It is ideal for use in very low power applications, such as sensor and metering devices, for measuring and monitoring purposes. A power down mode is included for additional power savings in such applications.

Designed as a general purpose device, the converter operates with rail-to-rail input voltages (positive differential). It operates from two separated unipolar power supplies, and provides an internal bandgap reference as common mode voltage source for the converter. The voltage reference is applied externally, typically from AVDD and AVSS.

The internal SAR controller enables operation with a wide clock frequency range of 32kHz up to 1MHz, while the resulting sample rate can be individually configured.

The IP core features an SPI interface for chip configuration and data acquisition. This interface provides a 100 word FIFO buffer enabling burst data transfer to the hosting controller.



Block diagram